Practitioner's Docket No.: CAT-00001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of (1st Inventor): Shashi B. Sakhuja
Assignee: Catalyst Semiconductor, Inc.
Serial No.: 10/656,982-9744 Group No.: 2816
Filed: 9/5/2003 Examiner: Terry L. Englund
For: "Progammable Analog Bias Circuits Using Floating Gate CMOS Technology"

November 30, 2004

VIA FACSIMILE - 703-872-9306
Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

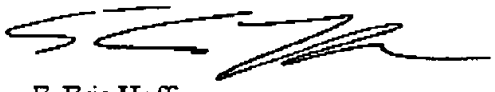
RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the outstanding Office Action dated November 3, 2004, in which the Examiner imposed a restriction requirement to election of invention for the above-referenced application, Applicant elects to prosecute the invention as in Group I, Claims 1 30 drawn to a : circuitry (or method) which includes at least two floating gate transistors, without traverse.

Applicant reserves the right to file divisional applications on the non-elected claims.

Respectfully submitted,



E. Eric Hoffman,
Reg. No. 38,186
Attorney for Applicant(s)

Customer No.: 022888
Tel. No.: (925) 895-3545
Fax No.: (925) 371-8186

CERTIFICATE OF TRANSMISSION (37 C.F.R. 1.8(a))

I hereby certify that, on the date shown below, this correspondence is being transmitted by facsimile to the Patent and Trademark Office.

Date: 11/30/04 Signature: Carrie Reddick